Customer No.: 31561
Application No.: 10/708,178
Docket No.: 10929-US-PA

AMENDMENT

In the Claims:

Please amend the claims as follows:

Claims 1-2 (canceled)

Claim 3 (currently amended) A driving stage for an LCD driving circuit, the driving stage being part of the LCD driving circuit in a cascade fashion, the driving stage comprising:

a clock input terminal, for receiving a clock signal having ~~one of~~ a first original level and a second original level;

a level shifter, coupling to the clock input terminal, for receiving the clock signal from the clock input terminal, operating at a first target level and a second target level, for amplifying the clock signal to a relay signal having a first relay level and a second relay level; and

an output buffer, coupling to the level shifter, for receiving the relay signal from the level shifter, operating at the first target level and the second target level, for amplifying the relay signal to a target signal having one of the first target level and the second target level,

wherein the first original level is higher than the second original level, the first target level is higher than the second target level, the first relay level is ~~between~~ higher

than the first original level and lower than the first target level, and the second relay level is ~~between~~ lower than the second original level and higher than the second target level.

Claims 4-7 (canceled)

Claim 8 (currently amended) The driving stage as recited in claim 3 further comprising a dynamic register, wherein the dynamic register couples to the clock input terminal, for receiving the clock signal, ~~to the level shifter,~~ and determines whether to ~~conduct the clock input terminal~~ provide the clock signal to the level shifter according to a control signal ~~module~~.

Claim 9 (currently amended) The driving stage as recited in claim 8, wherein the dynamic register comprises:

a register output terminal, coupling to the level shifter;

a first control signal input circuit, receiving a previous stage driving signal from a previous driving stage[[,]] and ~~determines~~ determining whether to conduct the clock ~~input terminal~~ signal to the register output terminal according to the previous stage driving signal; and

a second control signal input circuit, receiving a next stage driving signal from a next driving stage[[,]] and ~~determines~~ determining whether to conduct the register output terminal to the second target level according to the next stage driving signal.

Claim 10 (currently amended) The driving stage as recited in claim 8, wherein the dynamic register comprises:

a register output terminal, coupling to the level shifter;

a first control signal input circuit, receiving a previous stage driving signal from a previous driving stage[[,]] and ~~determines~~ determining whether to conduct the clock ~~input terminal~~ signal to the register output terminal according to the previous stage driving signal;

a second control signal input circuit, receiving the previous stage driving signal and output of the level shifter[[,]] and ~~determines~~ determining whether to conduct the driving stage to the second target level thereby.

Claim 11 (original) The driving stage as recited in claim 10 further comprising:

a level chopper, couples the first target level to the register output terminal, and determines whether to conduct the register output terminal to the first target level according to the previous stage driving signal.

Claim 12 (original) The driving stage as recited in claim 11, wherein the level chopper comprises p-type thin film transistor.